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Modified Booth Recoder for Efficient Add-Multiply Operator

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Abstract: Modified Booth algorithm has made multiplication easier. It consists of recoding table which has been used to minimize the partial products of multiplier. An adder and the multiplier operator of the unit is combine to form a single add-multiply unit. The fusion of the two operators resulting in Fused Add-Multiply(FAM) operator. In this paper different structured recoding techniques are used to implement the Modified Booth encoder incorporating in FAM. Along with the implementation of recoding techniques, comparison has been done with the existing and the designed Modified Booth recoder.

Keywords: Modified Booth Algorithm, adders, multipliers, add-multiply operation, arithmetic circuits, Xilinx.

I. INTRODUCTION

Electronic world consists of different applicative circuits for particular applications. These circuits comprises of complex arithmetic units. One such field is DSP(Digital Signal Processing) applications such as FFT (Fast Fourier transform), Filters(FIR-Finite Impulse Response),Signal Convolution and various other communication ,multimedia applications. The multiplier is the base of any arithmetic circuits. The multiplier consists of adders and shifters.

Multipliers were introduced to perform the multiplication operation of the arithmetic circuits using add and shift operation. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the whole system and also it is occupying more area consuming . Earlier multiplication was implemented via sequence of addition followed by subtraction and then shift operations [1]. An area-efficient parallel sign-magnitude multiplier that receives two N-bit numbers and produces an N-bit product, referred to as a truncated multiplier has been introduced[2].After some research it has been observed that the operations which share the data can be combined in the arithmetic circuits and performance can be increased[3]. The Multiply-Accumulator (MAC) and Multiply-Add (MAD) units were introduced as addition subsequent multiplication increasing the DSP processor's efficiency [4][5]. A novel reconfigurable low-power, high-performance matrix multiplier design has been presented showing a large reduction in power dissipation compared [6]. Any multiplier can be divided into three stages: Partial products generation stage these are generated by AND operation, partial products addition stage can be carried by different adders, and the final addition stage. An area efficient Wallace tree multiplier is designed using common Boolean logic based square root carry select adder [7].Many DSP applications are based on Add-Multiply operations which was designed by adding the bits and giving its output as an input to the multiplier. This increases the area and delay of the circuit[8]. In order to reduce the power consumption of multiplier, the low power Booth recoding methodology is implemented by recoding technique. This booth decoder will increase number of zeros in multiplicand. Booth multiplier has booth decoder to recode the given input to booth equivalent [9][1].For partial product generation, we propose a new modified Booth encoding (MBE) scheme to improve the performance of traditional MBE schemes[10]. To optimize the design of AM(Add-Multiply) operators the direct recoding of the sum of two numbers in its Modified Booth (MB) form are employed [11][12][13]. The direct recoding of the sum of two numbers in its MB form gives an efficient implementation of the fused Add-Multiply operator.

II. MODIFIED BOOTH RECODER

The modified-Booth algorithm is extensively used for high-speed multiplier circuits. Once, when array multipliers were used, the reduced number of generated partial products significantly improved multiplier performance. The Modified Booth Multiplier was proposed by O. L. Macsorley in 1961. The recoding method is widely used to generate the partial products for implementation of large parallel multipliers, which adopts the parallel encoding scheme . One of the solutions of realizing high speed multipliers is to enhance parallelism which
helps to decrease the number of subsequent stages. The original version of Booth algorithm (Radix-2) had two drawbacks:

- The number of add subtract operations and the number of shift operations becomes variable and becomes inconvenient in designing parallel multipliers.
- The algorithm becomes inefficient when there are isolated 1's.

These problems can be overcome by Modified Booth algorithm (MBA). In MBA process three bits at a time are recorded. Recoding the multiplier in higher radix is a powerful way to speed up standard Booth multiplication algorithm. In each cycle a greater number of bits can be inspected and eliminated therefore total number of cycles required to obtain products get reduced . Number of bits inspected in radix r is given by n = 1 + log2r. The Modified Booth algorithm is represented in the form :

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$$y_k^{MB} = -2y_{2k+1} + y_{2k} + y_{2k-1}$$

Table I. Modified Booth algorithm recoded table

Binary Inputs			Recoded Values	Operation to be performed
y_{2k+1}	y_{2k}	y_{2k-1}		
0	0	0	0	0*multiplicand
0	0	1	+1	+1*multiplicand
0	1	0	+1	+1*multiplicand
0	1	1	+2	+2*multiplicand
1	0	0	-2	-2*multiplicand
1	0	1	-1	-1*multiplicand
1	1	0	-1	-1*multiplicand
1	1	1	0	0*multiplicand

The architecture of the commonly used modified Booth multiplier consist of Booth encoder and decoder, Wallace tree and CLA. The inputs of the multiplier are multiplicand X and multiplier Y. The Booth encoder encodes input Y and derives the encoded signals. The Booth decoder generates the partial products using the encoded signals and the other input X. The Wallace tree computes the last two rows by adding the generated partial products. The last two rows are added to generate the final multiplication results using the carry look-ahead adder (CLA) [14].

III. PROPOSED IMPLEMENTATION

The proposed system fuses the adder unit with multiplier to implement Z= X(A+B) operation which uses the MB encoding technique where A and B are the inputs of the adder whose output Y is driven as an input to the multiplier along with the another input X as shown in a fig.1.The separate adder used in the conventional design adds a convincing delay to the critical path of the design.

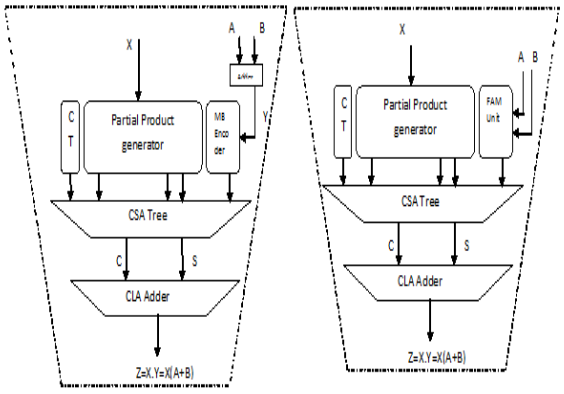

Fig.1 : Add-Multiply Operator (a) conventional AM operator (b) Fused Add-Multiply operator design where CT is the correction term,CSA tree is Carry Save Adder tree and CLA is Carry-Look Ahead Adder.

This critical path usually depends on the bit-width of the inputs due to the carry signals which propagates inside the adder. A use of Carry Look Ahead(CLA) adder is an option but it occupies more area and increases power consumption.

To optimize the AM operator design the adder unit is fused with MB encoding unit to form a single unit datapath. This is done by direct recoding of the sum Y=A+B to its MB form. This Fused Add-Multiply unit has only one adder at the end which results in a significant area reduction. The new techniques has been introduced to implement this fused add-multiply unit. In all techniques separate designs are implemented for an even and odd number of signed and unsigned bits.

(1) Technique I : FAM1

This technique uses two full adders to implement the design for odd and even width of bits stream. For the even number of bits two FAs are used as FA , a conventional full adder and FA* whose output value is given as:

$$FA^* = -2c_o + s = -q - q + c_i .$$

For odd bit-width an additional FA** is used at the end whose output value is

$$FA^{**} = -2c_o + s = -p - q + c_i .$$

(2) Technique II : FAM2

In this technique , for even bit-width a conventional full adder along with two half adders with the output value

$$HA^* = -2c + s = -p - q$$

are used whereas for odd width of bits an additional full adder as FA** has been used at the end.

(3) Technique III : FAM3

Here in this proposed scheme for even bit-width of input numbers a conventional full adder along with three different half adders has been used where the half adders are conventional HA,HA* and HA**.HA** output value is

$$HA^{**} = 2c - s = -p + q.$$

The odd bit-width input uses a conventional FA,HA and HA* along with and additional FA** at the end of the recoding scheme.

(4) Unsigned input :

For unsigned input numbers an additional conventional full adder, FA, is used at the end of the design along with the convetional FA,HA and HA*[1].

IV. EXPERIMENTAL WORK

Different recoding techniques has been designed using Xilinx ISE deign suite for all techniques and the output waveform has been shown in the below figures.

Comparison between the existing MB multiplier and the designed multiplier has been shown in the Table I.

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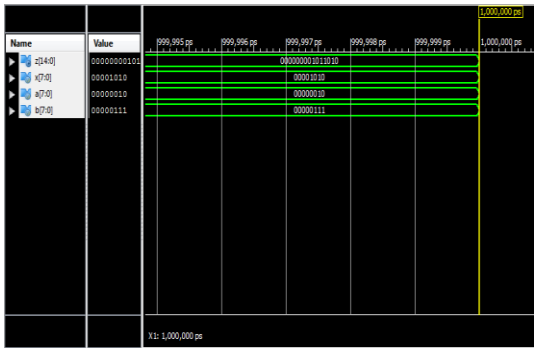

Fig. 2: unsigned FAM-even bit-width multiplier output waveform

Fig. 3: signed FAM-even bit-width multiplier output waveform

Fig. 4: unsigned FAM-odd bit-width multiplier output waveform

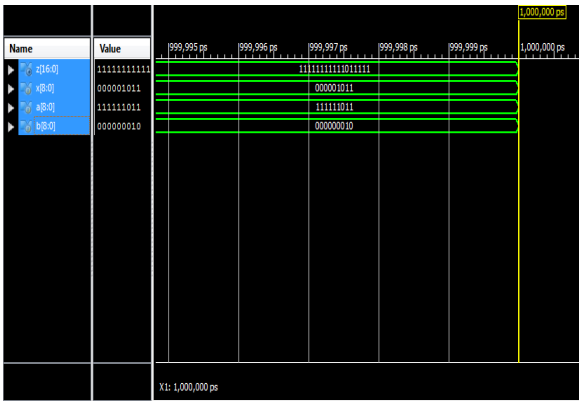

Fig.5 : signed FAM-odd bit-width multiplier output waveform

Table I. Comparison of existind and designed MB multiplier.

Comparison Table		
Parameters	**Existing MB**	**Designed MB**
Area	0.89 %	0.65%
Delay	14.28ns	9.29ns
Power	0.56W	0.034W

IV. CONCLUSION

This paper has focuses on the implementation of the Modified Booth Recoder by fusing the Add-Multiply operator. Different techniques has been used to implement the Fused Add-Multiply Operator by using different full adders and half adders whose output values has been given according to the signed and unsigned bit stream of the input numbers depending on the Modified Booth encoded table. The techniques has been designed for the odd and even bit- width of the input numbers. The comparison with the existing Modified Booth techniques has shown an effective optimizations in terms of delay,area and power.

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